First, looking at applicant's specification, the invention is directed to a silicon on insulator device with improved heat removal. As set forth in the Summary of the Invention on page 1, in accordance with the invention a semiconductor device is fabricated in a silicon on insulator (SOI) substrate including a supporting silicon substrate, a silicon oxide layer supported by the substrate and a silicon layer over the silicon oxide layer. More particularly, an electrical component, such as a transistor or capacitor, for example, is fabricated in the silicon layer over a portion of a silicon oxide layer, and then the portion of the substrate opposite from the component is masked and etched. A metal layer is then formed in the portion of the substrate which has been removed by etching with the metal layer providing heat removal from the component. The silicon oxide layer electrically insulates the metal layer from the semiconductor component.

Udrea discloses two embodiments of silicon on insulator (SOI) devices such as a power semiconductor device having an active region that includes a drift region, at least a portion of the drift region being provided in a membrane having opposed top and bottom surfaces, the top surface of the membrane having electrical terminals connected directly thereto to allow a voltage to be applied laterally across the drift region, the bottom surface of the membrane not having a semiconductor substrate positioned adjacent thereto. See paragraph [0019].

As stated in paragraph [0021] the drift region provided in the membrane having top and bottom surfaces also has at least one electrical terminal connected to the top surface and at least one electrical terminal connected to the bottom surface to allow a voltage to be applied vertically across the drift region.

For a first embodiment in which an electrical terminal is connected only to the top surface of the drift region, Udrea teaches the use of a heat sink layer 45 made of diamond, aluminum nitride, boron nitride or other materials with good electrically insulating properties and high thermal conductivity for the heat sink, which is applied to the bottom surface of the membrane not having a semiconductor substrate positioned adjacent thereto. See paragraph [0118] and figures 10A and 13C of Udrea, referenced by the Examiner. Clearly, the use of an insulating material as the heat sink as taught by Udrea is not a metal layer in the portion of the substrate in which silicon has been removed by etching as required in element c) of claim 15. The use of metal provides a much enhanced heat sink than would the electrically insulating materials specified by Udrea.

In a second embodiment of Udrea in which an electrical terminal is connected to the top surface of the membrane and an electrical terminal is connected directly to the bottom surface of the membrane to allow a voltage to be applied vertically across the drift region, as describe in paragraph [0021], Udrea describe in paragraph [0040] that the bottom terminal may be electrically and thermally conductive. The bottom terminal may be made of a metal or a combination of metals, such as aluminum, copper, etc. But in this embodiment, the metal layer provides the electrical terminal to the bottom surface of the membrane to allow a voltage to be applied vertically across the drift region. This is illustrated in Fig. 3B of the Udrea drawings and described in paragraph [0069] where electrical terminals 23 on the top surface and the bottom surface of the membrane provide potential lines.

In describing the example of Fig. 13C, paragraph [0079] states that the example is again of the SOI type having a silicon oxide insulating layer 50 and an electrically insulating but thermally conducting layer 45 deposited on the backside of the insulating layer.

Accordingly, it is seen that Udrea utilizes a metal bottom electrical terminal for applying a voltage directly to the semiconductor membrane and device, and in this regard is similar to the teachings of the cited Lin patent in which the bottom contact extends to the semiconductor device as an electrical terminal. These embodiments are unlike the claimed invention in providing an electrical terminal to the semiconductor device whereas in the claimed invention, the metal layer heat sink is electrically isolated from the semiconductor component by a silicon oxide layer.

For the foregoing reasons, it is respectfully submitted that the semiconductor on insulator semiconductor device as defined by claim 15 is patentable over Udrea under 35 USC § 102(e) or 103 and dependent claims 21-23 are patentable under 35 USC § 103(a) over Udrea in view of Lin. It is requested that claims 15 and 21-23 be allowed and the case advanced to issue. Should the Examiner have any question or comment regarding the present response, a telephone call to the undersigned attorney is requested.

If there are any issues remaining which the Examiner believes could be resolved through either a Supplemental Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

Applicants hereby petition for an extension of time which may be required to maintain the pendency of this case, and any required fee for such extension or any further fee required in

connection with the filing of this Amendment is to be charged to Deposit Account No. 500388 (Order No. CREEP027).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Henry K. Woodward
Reg. No. 22,672

P.O. Box 778
Berkeley, CA 94704-0778
(650) 314-5311 (direct line)